

Novel Buffer Design for Low Power and Less Delay in 45nm and 90nm Technology

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Abstract— Power dissipation and propagation delay are the predominant factor in buffer design when driving large capacitive loads. This paper proposes a novel buffer design called proposed buffer and also compares it with conventional buffer presently using in integrated circuits for two parameters, i.e. power dissipation and propagation delay. It is possible to achieve a reduction in power dissipation at optimized propagation delay by minimizing short circuit power and sub threshold leakage power which is predominant when supply voltage (V_{DD}) and threshold voltage (V_{th}) is minimized. The conventional as well as proposed buffer has been designed and simulated using Cadence Virtuoso tool in 45nm and 90nm technology. The end results show that proposed buffer design provides 28.8% and 11% reduction in power dissipation in 45nm and 90nm technology respectively. At same time propagation delay of proposed buffer when compared with conventional buffer increased by 40% and 25% in 45nm and 90nm technology respectively.

Keywords CMOS, VLSI, Buffer, nm

1. INTRODUCTION

As the scale of integration improves, more transistors, faster and smaller than their predecessors are being packed into chip. This leads to the steady growth of the operating frequency and processing capacity per chip, resulting in increased power dissipation. Another factor that fuels the needs for low power chips is the increased market demand for portable consumer electronics powered by batteries. The craving for smaller, lighter and more durable electronic products indirectly translates to low power requirements.

Buffers are widely used in many applications, to drive large capacitive loads in CMOS

integrated circuits at high speed, while ensuring that the load placed on previous stages of the signal path is not too large, in the memory access path as word-line drivers, to drive large off-chip capacitances in I/O circuits, and in clock trees to ensure that skew constraints are satisfied. But, deployment of these buffers in high-performance systems imposes a power overhead on each instance regardless to its actual performance.

Now the attention of many people is in high-performance VLSI design because of emerging need for miniaturization, and hence designs optimization for trading-off power and performance in nanometer scale integrated circuits. The power consumption can be reduced by either supply voltage V_{DD} or threshold voltage V_{th} . Decreasing the V_{th} not only increases leakage power but also short circuit power. In total power dissipation, 30 to 50% share is only because of leakage current and short circuit current. To reduce short circuit power and leakage power, a novel buffer design has been proposed in this paper.

Section 2 discusses conventional buffer and its design aspects and Section 3 discusses proposed buffer. Section 4 reports results and discussions, conclusion on section 5 and References in section 6.

2. CMOS CONVENTIONAL BUFFER DESIGN.

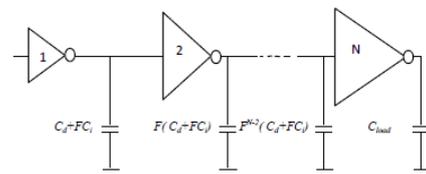


Figure 1 conventional buffer

The buffer consists of a chain of inverter stages where width of each MOS transistor in a stage is increased by a constant factor (called taper factor) than that of the

transistors in the previous stage. The constant increase in width of transistors in each stage provides fixed ratio of output current drive to output capacitance and hence equal rise, fall, and delay times for each stage. Here C_i denotes the input capacitance of minimum size inverter, C_d denotes the drain capacitance of minimum size inverter, C_{load} denotes the load capacitance of the last stage inverter, N denotes number of stages in the buffer chain and F denotes the scaling factor per stage in the inverter buffer chain.

A large inverter is required to drive the large capacitive load at final stage. Because the gate capacitance of inverter is proportional to its size, a medium inverter is required to drive a larger inverter. The number of buffer stages required in each of the two design conditions depends on technology dependent tapering factor F .

$$F^N = C_d / C_i$$

To achieve minimum delay the numbers of stages required are given by,

$$N_D = \ln(C_L / C_i) / \ln(F)$$

The power dissipation of the succeeding inverter increases F times compared to that of preceding inverter

$$P_i = F P_{i-1}$$

2.1 Sources of Power Consumption

Dynamic Power Consumption

Dynamic power consumption is the most significant source of dynamic power dissipation in CMOS circuit due to charging and discharging of capacitance. The capacitance forms due to parasitic effects of interconnections wires and transistors. Such parasitic capacitance cannot be avoided and it has a significant impact on power dissipation of circuits.

$$P_{dyn} = f C_L V_{dd}$$

Short Circuit Power Consumption.

When input signal level is above V_{tn} NMOS is on and when input is below V_{tp} the PMOS is on. There is a short duration in which the input level is between V_{tn} and V_{tp} and both the transistors are on. This causes short circuit current from V_{DD} to ground and dissipates power. The electrical energy drawn from source is dissipated as heat in

the P and N transistors.

$$P_{short} = \frac{\beta r}{9.6T} (V_{DD} - 2V_m)^3$$

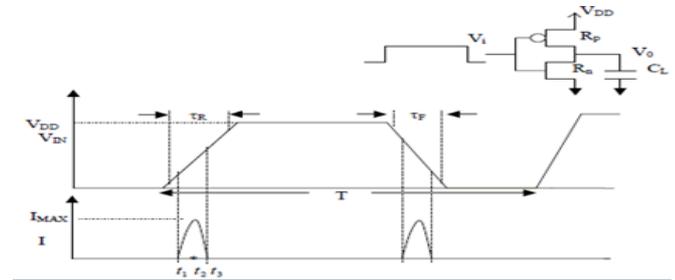


Figure 2 Short circuit current

Static Power Consumption

Ideally, CMOS circuits dissipates no static (DC) power since in the steady state no direct path from V_{dd} to ground. Of course this scenario can never be realized in practice since in reality the MOS transistor is not a perfect switch. Thus, there give rise to a static component of CMOS power dissipation.

$$P_{stat} = V_{dd} (I_{don} + I_{dop}) / 2$$

Total Power

Total power is the sum of dynamic, static and short circuit power consumption; the equation is given by-

$$P_{total} = P_{dyn} + P_{stat} + P_{short}$$

2.2 Circuit Diagram of Conventional buffer

A 4 stage conventional buffer is shown in figure 2 and figure3, which has capacitive load $C_L = 150\text{fF}$ and $F = 3$ when designed for minimum delay condition. The input is applied at I_N and different buffer stages are cascaded to get output across C_L .

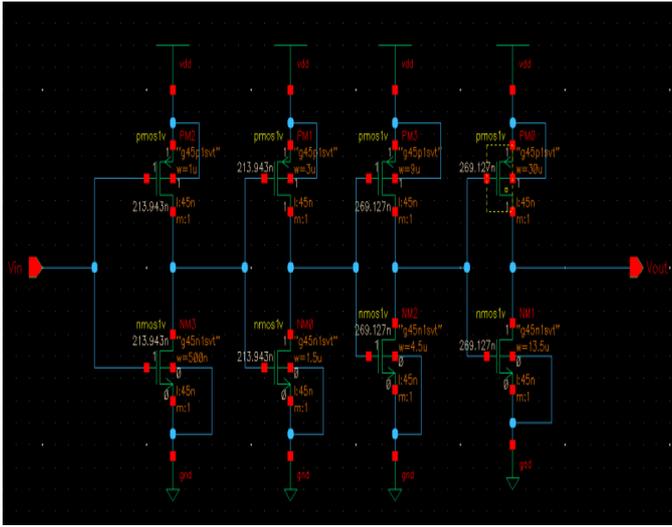


Figure 3 Circuit diagram of conventional buffer

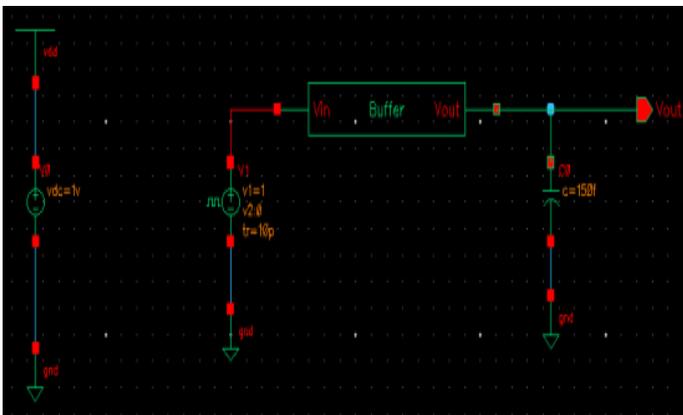


Figure 4 Test bench for Conventional buffer

3. Proposed buffer

Most of the power dissipation in CMOS structures is caused by charging/discharging the output load and by the short-circuit current that flows from the power supply to the ground, during switching of structures. The significance of short-circuit power dissipation in CMOS buffers is due to on-chip and off-chip signal driver circuits.

It is important to reduce short circuit power dissipation. The proposed buffer dissipates less power because the short circuit component of power is eliminated in the design before every output signal transition by tri-stating its output node momentarily. This is achieved by applying the gate driving signal of PMOS (NMOS) transistor to NMOS (PMOS) transistor of the output stage through a feedback network which delays the driving signal and avoids simultaneous turn on of NMOS and

PMOS transistors during signal transition which is the very cause of short circuit current. Further, the capacitive load dependent tapering factor is applied to all the stages including the final stage.

Below figure shows a 4 stage proposed taper buffer in which input signal is applied at IN which is amplified by 1st and 2nd stage. The feedback network is applied in 3rd and 4th stage, where T1, T4, T5, T7 are PMOS transistors and T2, T3, T6, T8 are NMOS transistors. INV1 and INV2 are minimum sized inverters which are connected to gate terminals of T8 and T7 for their input and with T2 and T5 as output respectively. The output of 2nd stage is connected to T1, T3, T4 and T6 only. INV2 which turns off transistor T5. Thus gate terminal of T8 cannot charge until gate terminal of T7 charges to logic high.

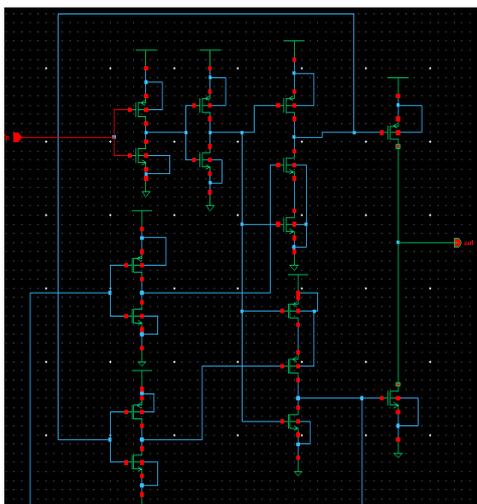
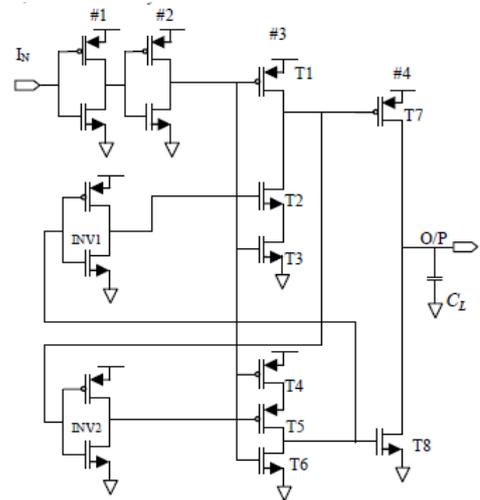
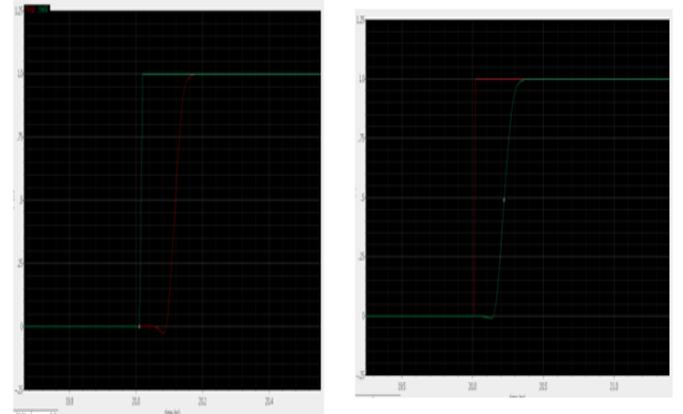
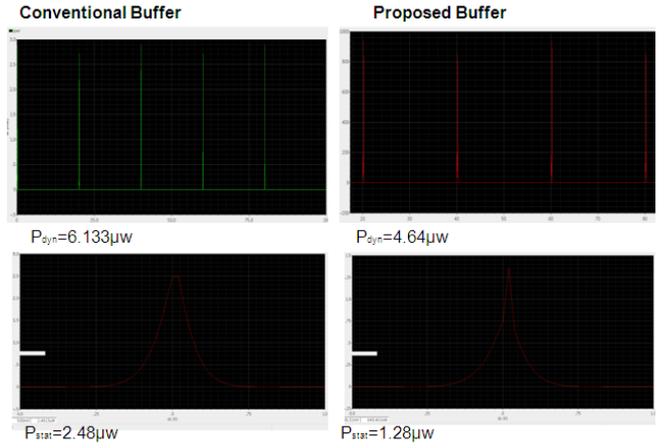


Figure 5 circuit diagram of proposed buffer

Now assuming that input signal made a transition from a logic high level to a logic low level, transistors T1 and T4 turn on, and transistors T3 and T6 turn off. As a result, gate terminal of T7 charges first to logic high and gate terminal of T8 starts charging after gate terminal of T7 is charged to logic high. Thus, charging of gate terminal of T8 is delayed which may cause a delay in turn on of transistor T8. Similarly, when input signal makes a transition from a logic low to high, gate terminal of T8 discharges first and then gate terminal T7 is discharged. Again, the delay in discharge of gate terminal of T7 may cause delay in turn on of transistor T7. The delay in charging/discharging of gate terminals of T7 and T8 may avoid these transistors being on at the same time and thus reduces the short circuit power dissipation.

4. Results and discussions.

Computations have been made analytically for parameters like number of stages, taper factor etc. and then simulation in 45 nm technology and 90 nm technology node is performed for conventional CMOS tapered buffer as well as for proposed taper buffer designs using Cadence Virtuoso tool and power estimation done using Result browser. Both the designs are compared and contrasted for performance metrics such as power dissipation and propagation delay.

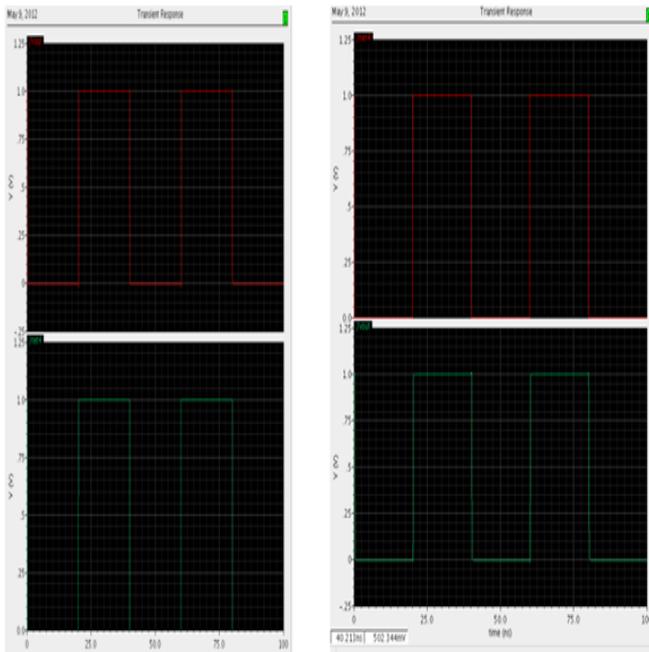


Delay=0.12nsec

Delay=0.2nsec

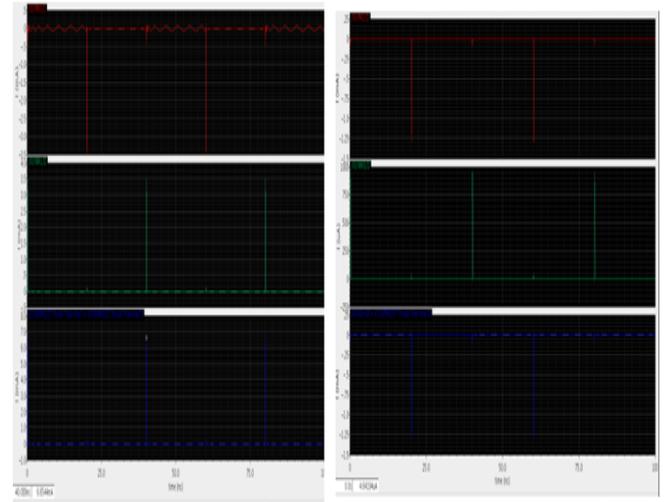
Conventional Buffer

Proposed Buffer



Conventional Buffer

Proposed Buffer



I_{short}=10.59µA

I_{short}=1.394µA

Results in 45nm Technology

ACKNOWLEDGEMENT

Table 1 45nm technology results

| C _L (fF) | F | Conventional Buffer | | Proposed Buffer | | % increase in propagation delay | % decrease in Power dissipation |
|------------------------|---|-----------------------|-----------------------|-----------------------|-----------------------|---------------------------------|---------------------------------|
| | | (ns) | | (uW) | | | |
| | | Propagation delay(ns) | Power Dissipation(uW) | Propagation delay(ns) | Power Dissipation(uW) | | |
| 150 | 3 | 0.12 | 8.613 | 0.2 | 5.92 | 40 | 28.8 |

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Results in 90nm Technology

Table 2 90nm technology results

| C _L (fF) | F | Conventional Buffer | | Proposed Buffer | | % increase in propagation delay | % decrease in Power dissipation |
|------------------------|---|-----------------------|-----------------------|-----------------------|-----------------------|---------------------------------|---------------------------------|
| | | (ns) | | (uW) | | | |
| | | Propagation delay(ns) | Power Dissipation(uW) | Propagation delay(ns) | Power Dissipation(uW) | | |
| 150 | 3 | 0.15 | 271.75 | 0.2 | 241.7 | 25 | 11 |

5. CONCLUSION

In this paper power dissipation and propagation delay parameters have been optimized during design of CMOS buffer driving large capacitive loads. The short circuit power and sub threshold leakage power have been minimized to reduce total power dissipation in deep submicron (DSM) region. The proposed buffer has been designed in 45 nm technology and 90 nm technology node and simulated in Cadence virtuoso tool. An improvement of **28.8% and 11%** in power dissipation has been achieved in 45 nm technology and 90 nm technology respectively. Hence, the proposed buffer can be used to provide power efficient solutions for portable VLSI applications at optimum propagation delay.