Design of 14-Bit Cyclic Vernier Ring Time-to-Digital Converter

Mahesha N.B
Assistant Professor at Rai technology University
nbmahesh512@gmail.com

Abstract. Time to digital converter is used to digitize the delay difference between two signals. In this paper, an implementation of 14 bit, 10 ps Vernier Ring Time to Digital Converter (VRTDC) is presented, which places the Vernier delay cells and arbiters in a ring format and reuses them for the measurement of the input time interval. A pre-logic unit is developed to decide leading and lagging signals, through which it is possible to measure both positive and negative phase difference. It is possible to achieve large detectable range, fine time measurement, small die size and low power consumption with the proposed VRTDC. The design is modeled using Verilog and synthesized using RTL Compiler targeting the design to 180nm standard cell library.

Keywords: Vernier ring, VRTDC, Time-to-digital converter, TDC, Frequency synthesis.

1 Introduction

Time to digital converter is an indispensible system block of many sensitive instruments which measure phase difference between two signals. It can also be used to recognize events and provide a digital representation of the time at which they occur. For example, a TDC might output the time of arrival for each incoming pulse. Some applications measure the time interval and convert it into digital output. TDCs find applications in many physical experiments, like time-of-flight and life time measurements in atomic and high energy physics.

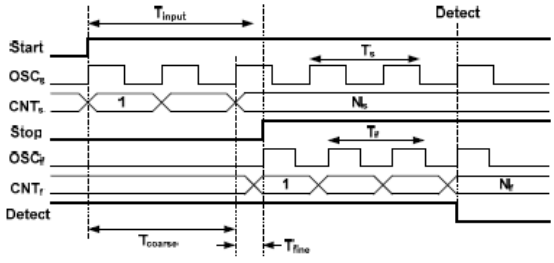


Fig. 1. Measurement of time difference using TDC

TDCs are used in large amount of applications, where the time interval between two signal pulses (start and stop pulse) should be determined. Measurement is started or stopped when either the rising or the falling edge of signal crosses the threshold.

An inverter-chain based TDC was employed in the first implemented for a blue-tooth radio application [3]. Since then, a variety of TDC architectures have been proposed with improved resolution and detectable range. Although there are many ways to digitize the input time interval, the digital inverter-delay-line is still an appealing structure due to its digital-intensive design approach.

The proposed TDC is implemented as a digital system block, as such implementation offers benefits like decrease in die area, high frequency operation, low power consumption and less sensitive to process, voltage and temperature variations.Fig.2(a) shows the conventional inverter delay line based TDC. Its time resolution is the propagation delay of each individual inverter, while its detectable range is proportional to the number of delay stages used.

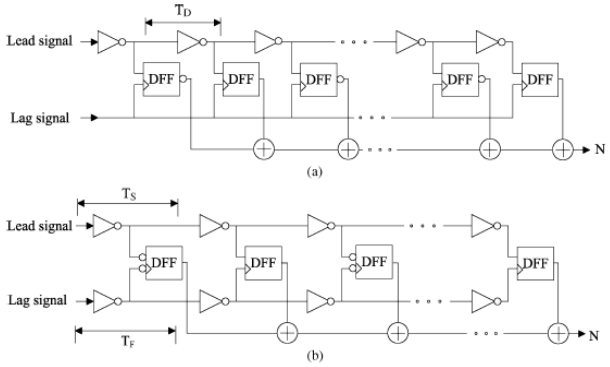


Fig. 2. Vernier delay line using (a) single and (b) two inverter chains.

A Vernier delay line is well known for its fine time resolution [4]. Figure 2(b) illustrates a simplified Vernier inverter delay line TDC. It employs two inverter/buffer chains with different delays of T_s and T_f , respectively. Time resolution of the Vernier TDC now becomes the delay difference of two delay lines, namely, T_s-T_f. where T_S and T_f are delay of slow and fast inverter cells respectively.

Some of TDC architectures have been compared with respect to Resolution and detectable range. Table 1 gives the comparison of different TDC architectures. A multipath gated ring oscillator (GRO)- GRO-based TDC achieves a detectable range of 11 bits [5]. A two-level interpolation TDC with this parallel structure achieved a time resolution of 12.2 ps in a 0.35µm CMOS technology [6].

Table 1. Comparison of different TDC architectures

Reference	[3]	[4]	[5]	[6]	This paper
Time Resolution (ps)	24	20	6	12.2	10
Measurement Range in bits	8	5	11	14	12

In the proposed work, Vernier delay cells are placed in a ring format such that the delay chains can be reused for measuring large time intervals. Coarse and fine counters are used to monitor the number of laps, the signals propagate along the ring. Arbiters are used to record the location where the lag signal catches up with the lead signal.

This paper is organized as follows: Section 2 gives implementation of critical building blocks of the VRTDC. Vernier ring Time to digital converter implementation is presented in Section 3. Results and conclusion are presented in section 4 and references are presented in section 5.

2 Vernier Ring Time to Digital Converter (VRTDC) System

The architecture of 14-bit VRTDC system composed of the VRTDC core, pre-logic unit, and thermometer - to -binary encoder, 7-bit fine counter and 7-bit coarse counter which is shown in figure 3.

The outputs of 30 arbiters are combined to form 30-bit thermometer code “TH ” and are translated into a 4-bit binary code by a thermometer-to-binary encoder. The total amount of delay is composed of four elements: the sign bit, the coarse counter value, the fine counter value and the thermometer code.

$$N = \pm 30\,(Nf\text{-}Nc)+TH+30\,NCts/R$$

where N is the TDC output, NC is the coarse counter output, Nf is the fine counter output, TH is thermometer-to-binary encoder output, ts is the sampling time and R is the resolution.

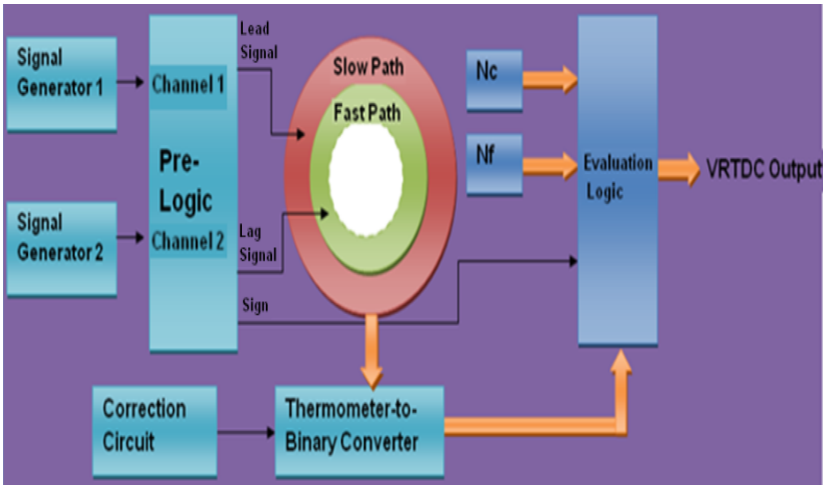


Fig. 2. VRTDC Architecture

3 VRTDC Implementation

The detailed description of the VRTDC architecture which consists of pre-logic unit, two types of arbiters with edge detectors, the thermometer-to-binary encoder and correction circuit is presented in this section.

3.1 Pre-logic Unit

The reference and feedback signals are applied to the Pre-logic unit , the lead signal is steered to the slow ring, while the lag signal goes to the fast ring.

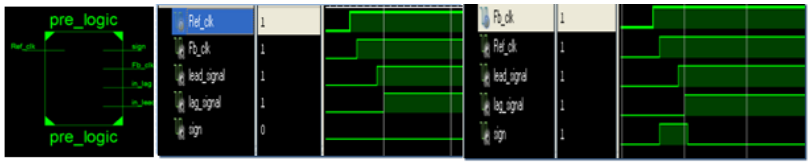
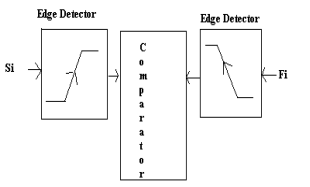


Fig. 3. Pre-logic Unit indicating positive and negative phase differences

It consists of delay path, multiplexers,arbiter and reset path. Arbiter decides the sign bit and multiplexers guide the lead signal to slow ring and lag signal to fast ring.

3.2 Arbiters and Edge Detectors

Arbiter A and Arbiter B are triggered by rising and falling edges respectively, uses respective edge detectors. Earlier implementations TDC have transistor based arbiters. This work proposes fully digital implementation as figure 4 and 5.



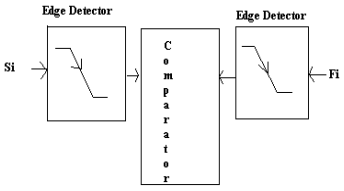
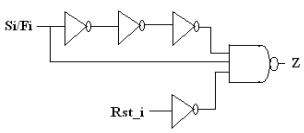


Fig. 4. Arbiter A

Fig 6: Arbiter B



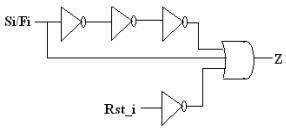


Fig. 7. Rising Edge Detector

Fig 8: Falling Edge Detector

When lag signal catches the lead signal, the arbiter outputs high. Two

sets of a arbiters works alternatively in odd and even laps.

Fig. 9. Arbiter A and Arbiter B simulation

3.3 Thermometer-to- binary encoder

When lag signal catches the lead signal arbiter outputs "1".The output of all 30-arbiters are combined to form Thermometer code "TH". This 30-bit Thermometer code is converted to 4-bit binary code using Thermometer-binary encoder, as shown below.

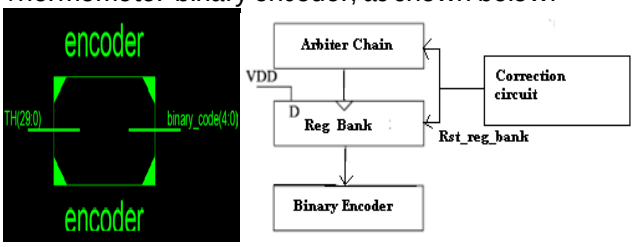


Fig. 9. Thermometer-to-binary encoder

3.4 Correction circuit

In the process of chasing lead signal by the lag signal , an unexpected "01" transition may occur as shown below. Edge C is supposed to be compared with edge a. Unfortunately the edge is going to be compared with the next falling edge at b. Arbiter B(1) and the following few arbiters will be set to "1". Moreover, arbiter A15 and B14 have been set to "0" before lag signal propagates in the fast ring. A "001" transition will be erroneously detected at the least significant bit of thermometer code. The VRTDC would have mistakenly judged that the lag signal had caught up with the lead signal without proper error detection.

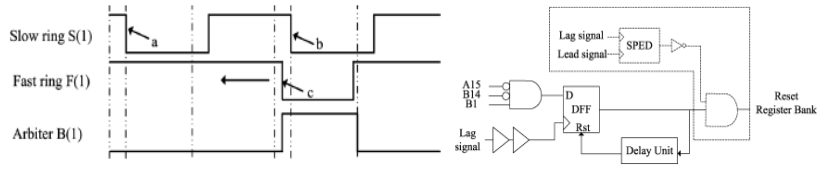


Fig. 11. Correction circuit [1]

Fig12: Correction circuit[1]

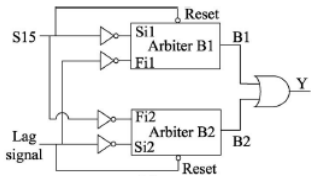


Fig. 13. SPED [1](Small Phase Error Detection)

The correction circuit will screen the "001" detection signal and keep edge c of the lag signal chasing edge a till the next catch-up happens. Small phase error detection circuit is used to measure the minute phase difference (<<0.2ps).

3.5 Course and Fine Counters

Before lag signal enters the ring, VRTDC will be working in the course measurement mode which measures number of periods lead signal is ahead lag signal(Nc), and when lag signal enters, it switches to fine measurement which measures fraction of the period delay difference.

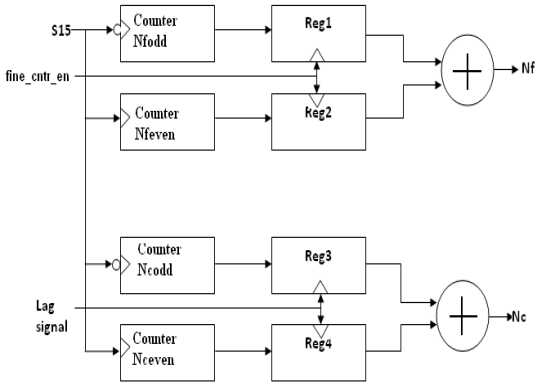


Fig. 14. Counter

4 Results and conclusion

Proposed VRTDC was synthesized separately using RTL compiler and Xilinx ISE. The design was targeted to 180 nm standard cell library in RTL Compiler. The synthesis report is as given below.

Instance	Cells	Leakage Power(nW)	Dynamic Power(nW)	Total Power(nW)
VRTDC	627	38548.183	79146.81	117694.993

Instance	Cells	Cell Area
VRTDC	627	5067

The simulation results have indicated 10 ps resolution for 14 bit measurement.

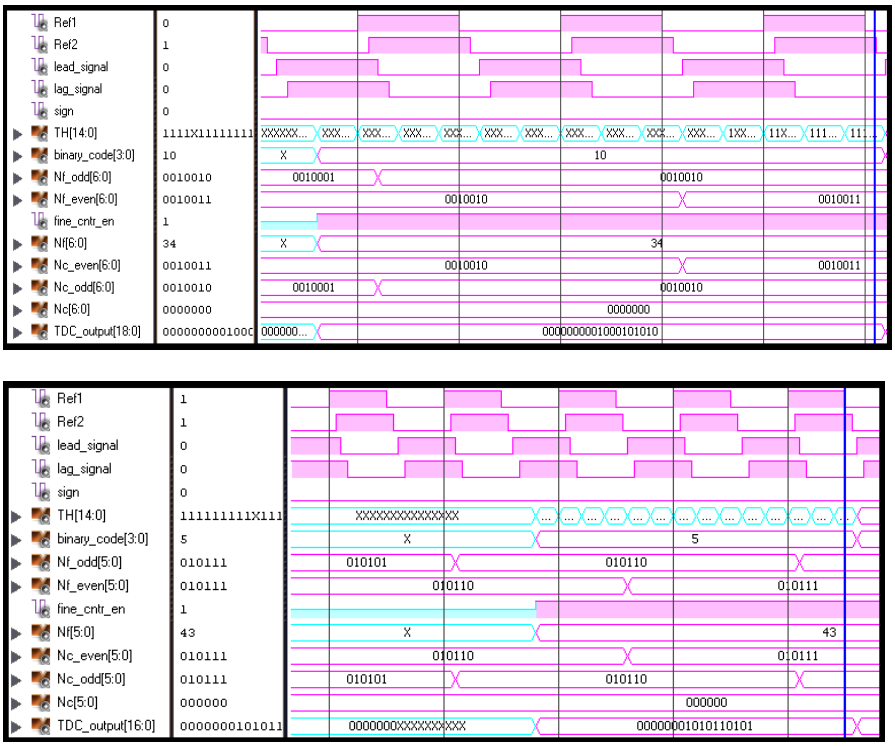


Fig. **15.** Simulation results of VRTDC at different times

5 References

1. Jianjun Yu, Fa Foster Dai,Richard C.Jaeger *"A 12-bit Vernier Ring Time-to-digital converter n 0.13um CMOS Technology"* IEEE journal of solid state circuits. VOL 45 No4 April2010.

2. Youngmin Park and David D. Wentzloff *"A Cyclic Vernier Time-to-Digital Converter Synthesized from a 65nm CMOS Standard Library"* ©2010 IEEE.

3. R. B. Staszewski, C. M. Hung, K. Maggio, J.Wallberg, D. Leipold, and P. T. Balsara, *"All-digital phase-domain TX frequency synthesizer for bluetooth radios in 0.13 umCMOS,"* in IEEE ISSCC Dig. Tech. Papers,Feb. 2004, vol. 1, pp. 272–527.

4. P.Dudek, S.SzcZepanski,and J.Hatfield, *" A high resolution CMOS time to digital converter utilizing a vernier delay line",*IEEE J Solid-state circuits , vol.35, no2,pp.240u247,Feb2000.

5. M.Z.Straayer and M.H perrot, *"An efficient high-resolution 11-bit noise-shaping multi-path gated ring oscillator TDC"*, in symp, VLSI circuits Dig. Tech. papers. june 2008. Pp.82-83.

6. V. Ramakrishnan and P. T. Balsara, *"A wide-range, high-resolution, compact CMOS time to digital converter,"* in *Proc. 19th Int. Conf. VLSI Design (VLSID'06)*, Jan. 2006, p. 6.

adfa, p. 9, 2011.